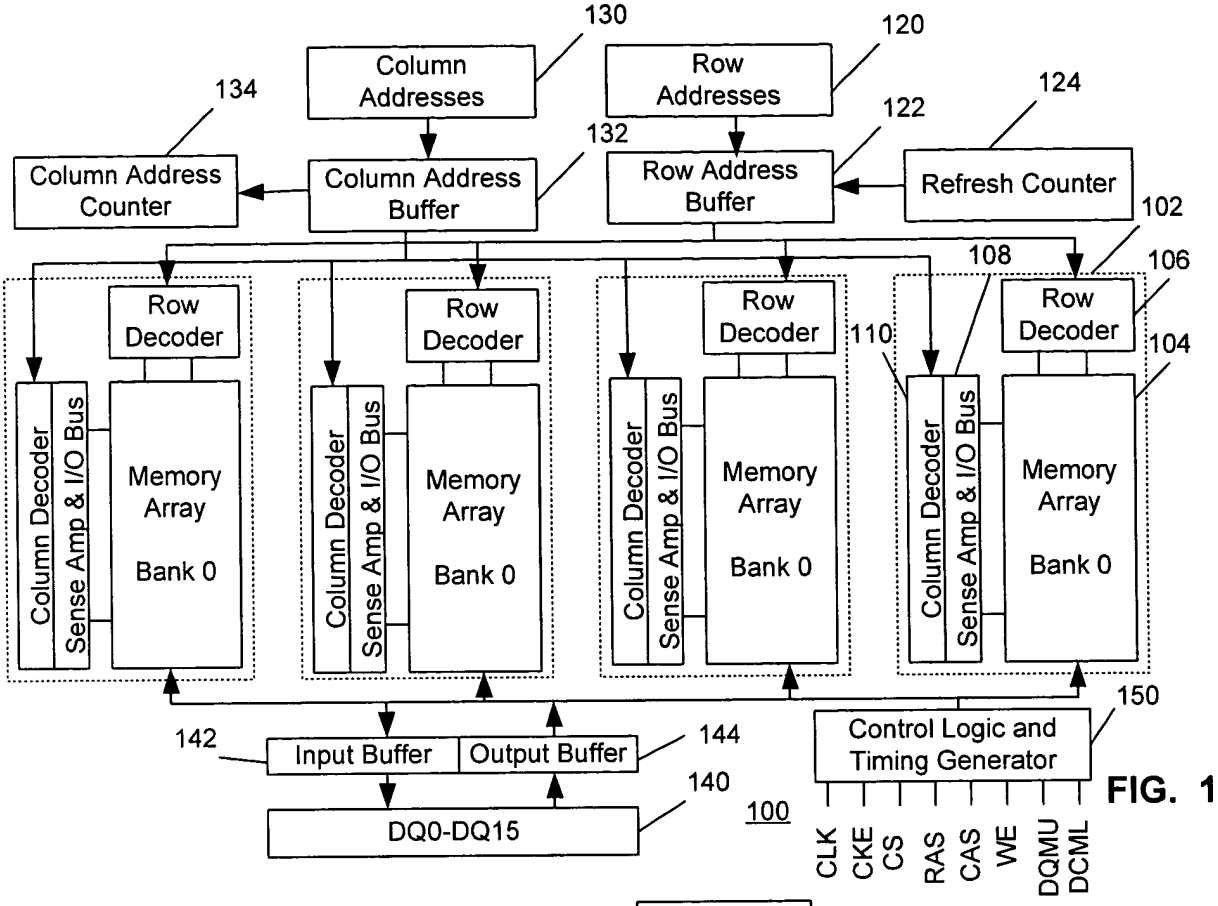
130
Column Addresses
120
Row Addresses
134
Column Address Counter
132
Column Address Buffer
122
Row Address Buffer
124
Refresh Counter
102
108
106
Row Decoder
Column Decoder
Sense Amp & I/O Bus
Memory Array
Bank 0
110
104
150
142
Input Buffer
Output Buffer
144
140
DQ0-DQ15
100
Control Logic and Timing Generator
CLK
CKE
CS
RAS
CAS
WE
DQMU
DCML

FIG. 1

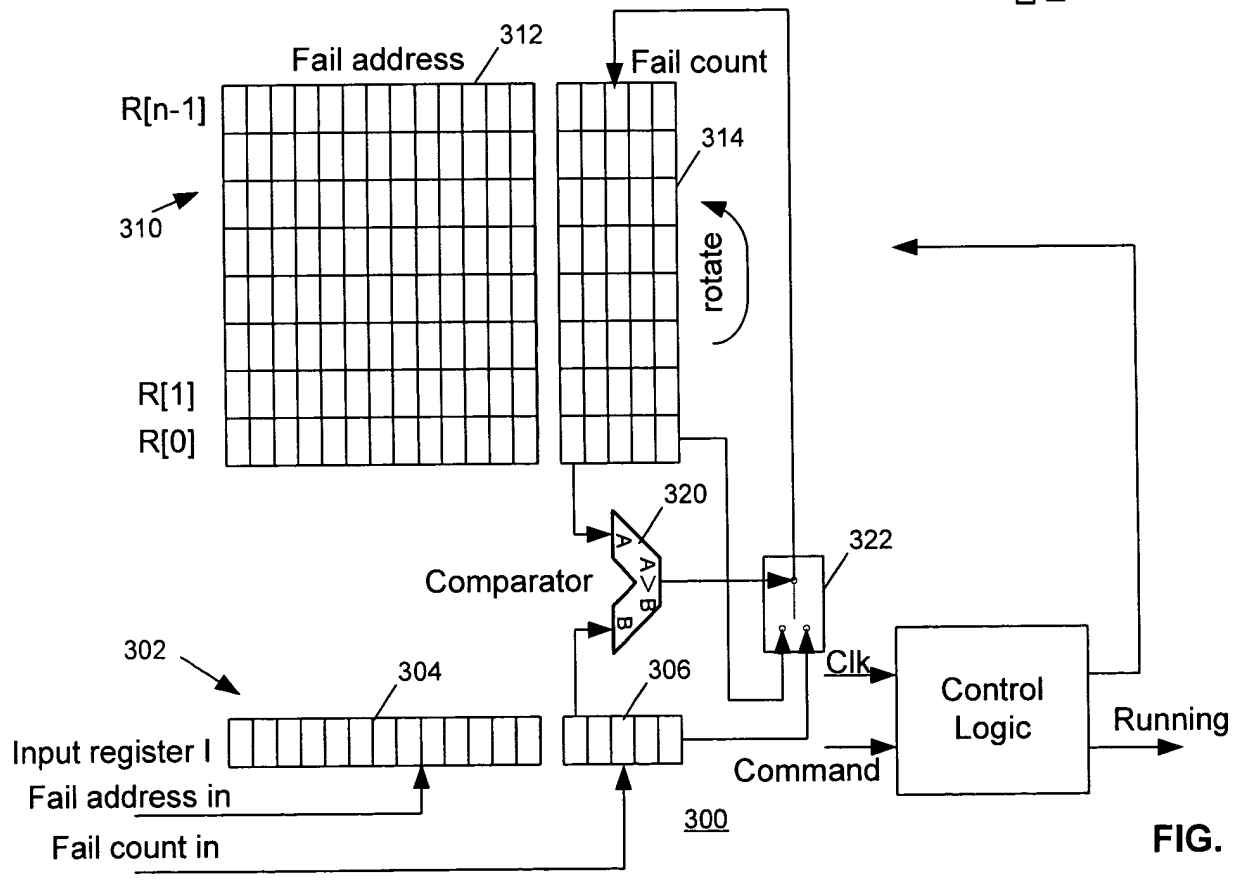
312
Fail address
Fail count
R[n-1]
314
310
rotate
R[1]
R[0]
320
Comparator
A
A>B
B
322
302
304
306
Clk
Control Logic
Running
Input register I
Command
Fail address in
300
Fail count in

FIG. 3

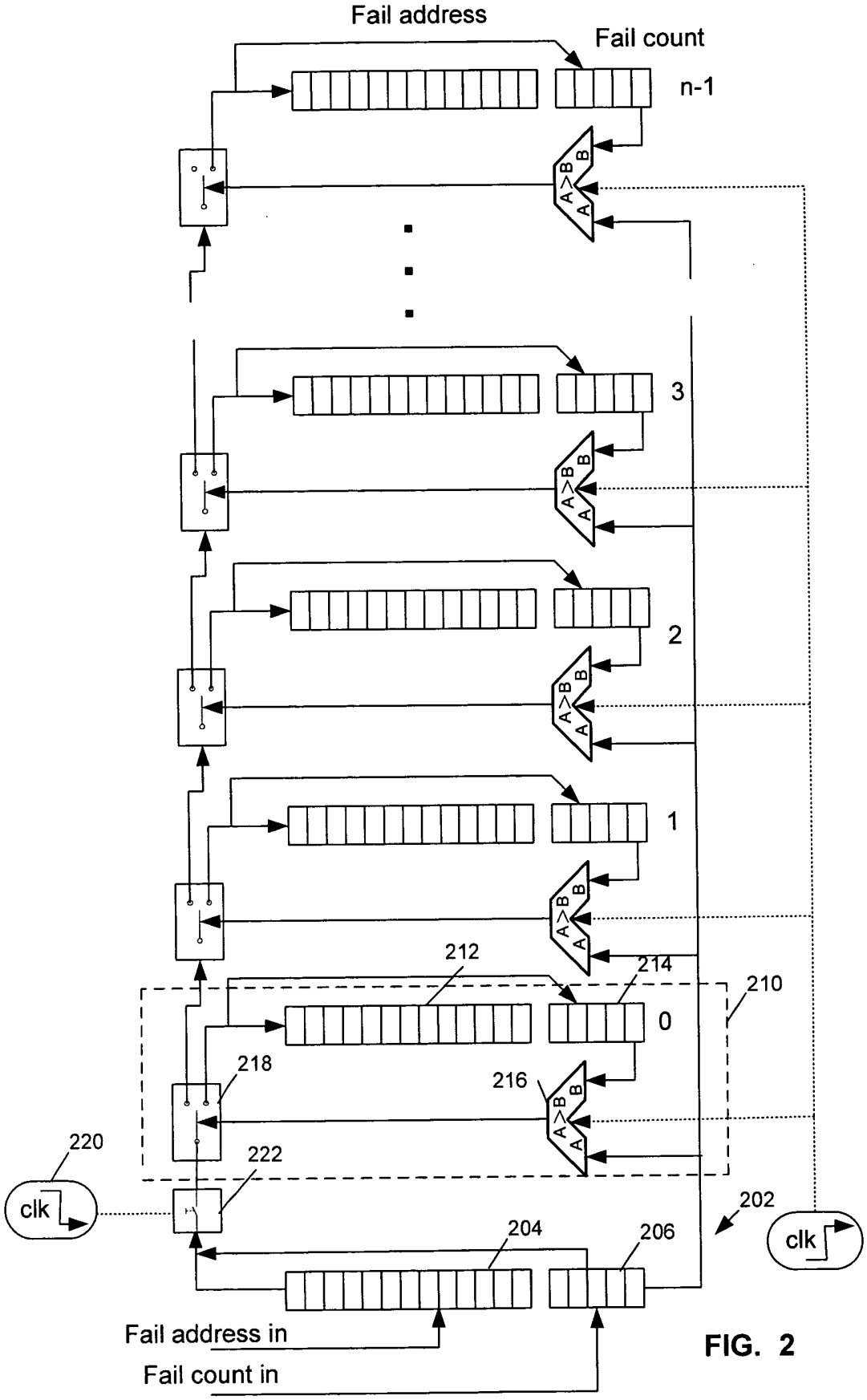
Fail address
Fail count
n-1
3
2
1
0
212
214
210
218
216
220
222
clk
202
clk
204
206
Fail address in
Fail count in

FIG. 2

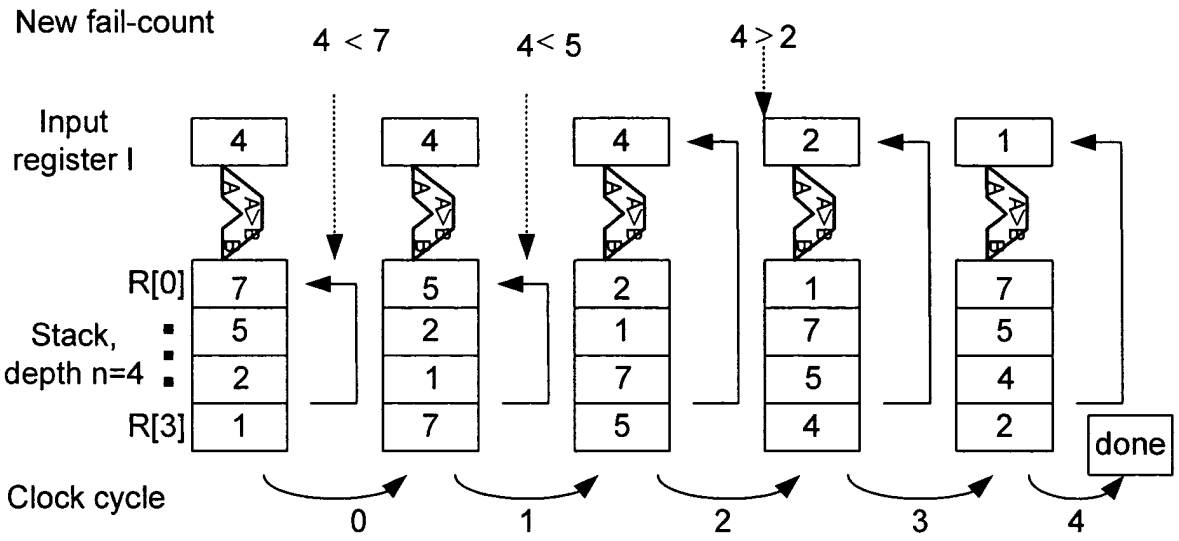
New fail-count
4 < 7
4< 5
4 > 2
Input register I
4
4
4
2
1
R[0]
7
5
2
1
7
Stack, depth n=4
5
2
1
7
5
4
4
R[3]
1
7
5
4
2
done
Clock cycle
0
1
2
3
4

FIG. 4

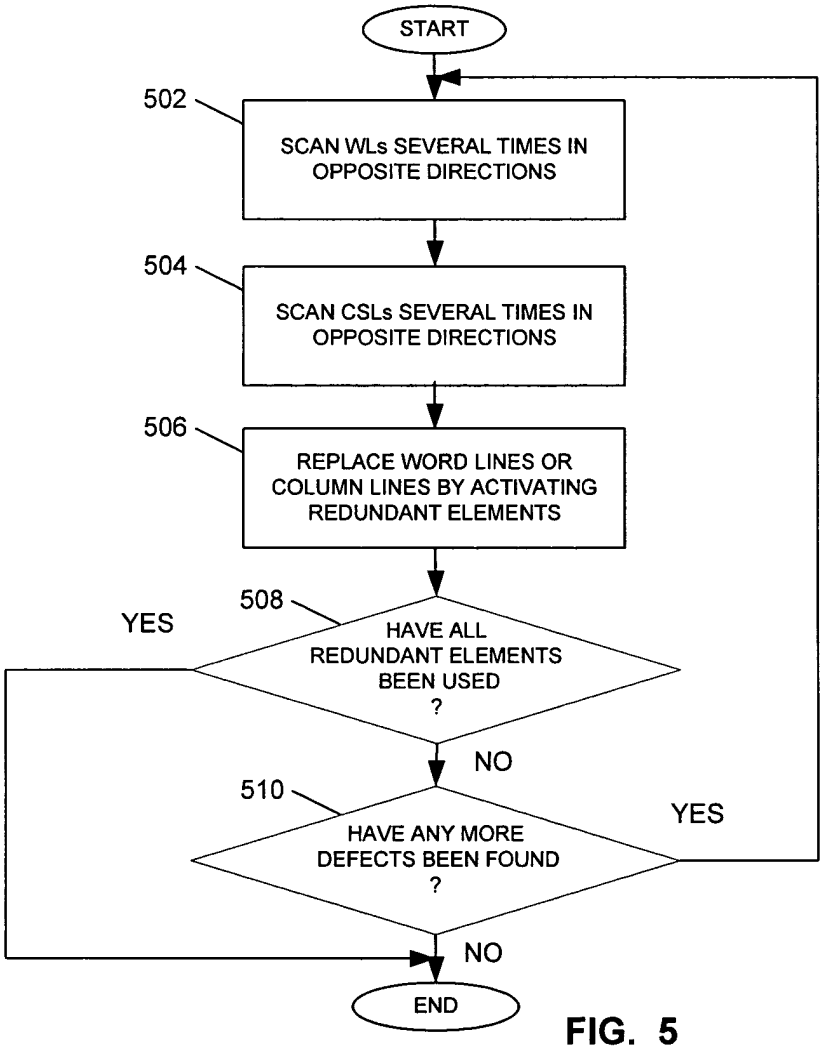
START
502
SCAN WLs SEVERAL TIMES IN OPPOSITE DIRECTIONS
504
SCAN CSLs SEVERAL TIMES IN OPPOSITE DIRECTIONS
506
REPLACE WORD LINES OR COLUMN LINES BY ACTIVATING REDUNDANT ELEMENTS
508
HAVE ALL REDUNDANT ELEMENTS BEEN USED ?
YES
NO
510
HAVE ANY MORE DEFECTS BEEN FOUND ?
YES
NO
END

FIG. 5

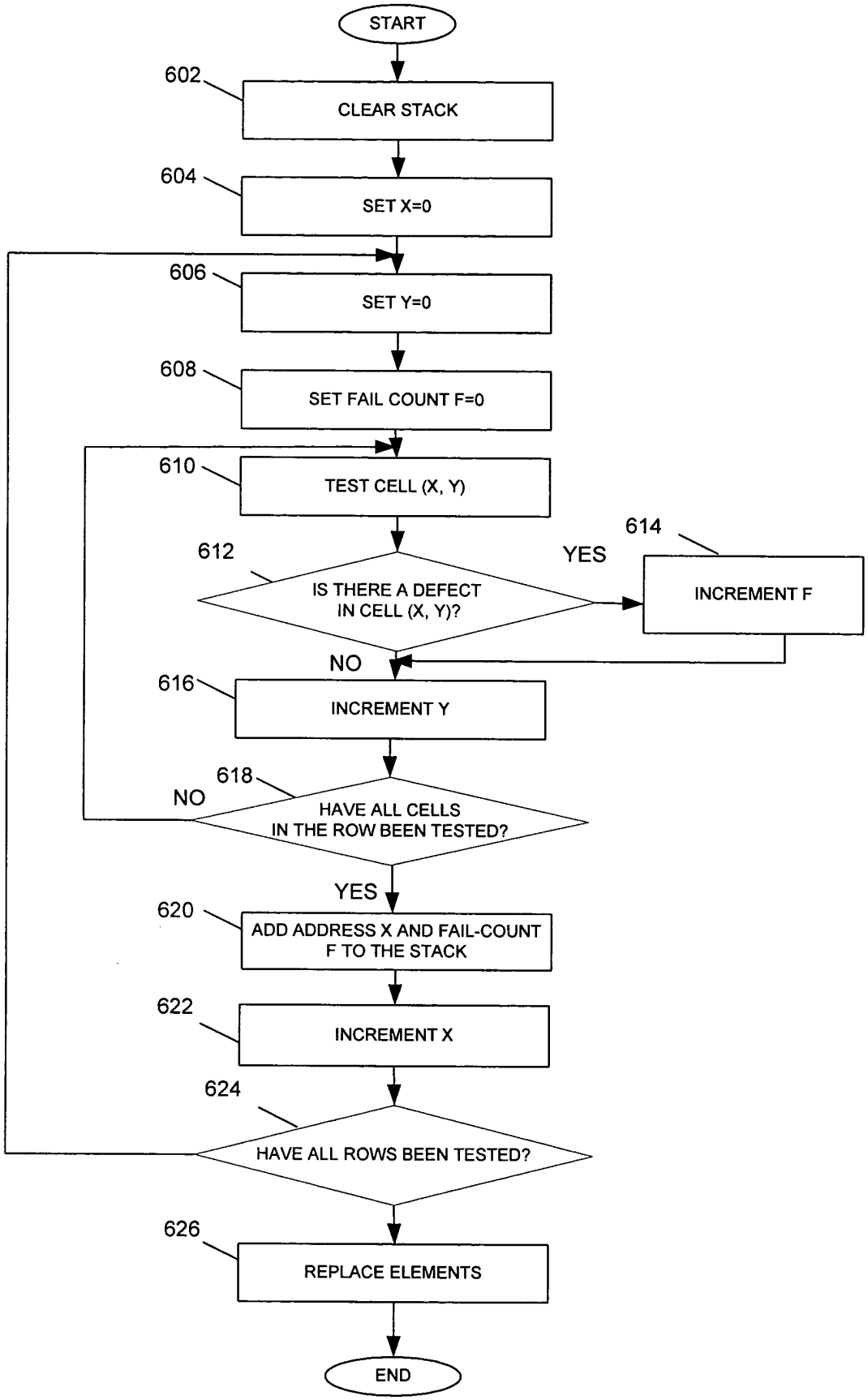
START
602
CLEAR STACK
604
SET X=0
606
SET Y=0
608
SET FAIL COUNT F=0
610
TEST CELL (X, Y)
612
IS THERE A DEFECT IN CELL (X, Y)?
YES
614
INCREMENT F
NO
616
INCREMENT Y
618
NO
HAVE ALL CELLS IN THE ROW BEEN TESTED?
YES
620
ADD ADDRESS X AND FAIL-COUNT F TO THE STACK
622
INCREMENT X
624
HAVE ALL ROWS BEEN TESTED?
626
REPLACE ELEMENTS
END

FIG. 6

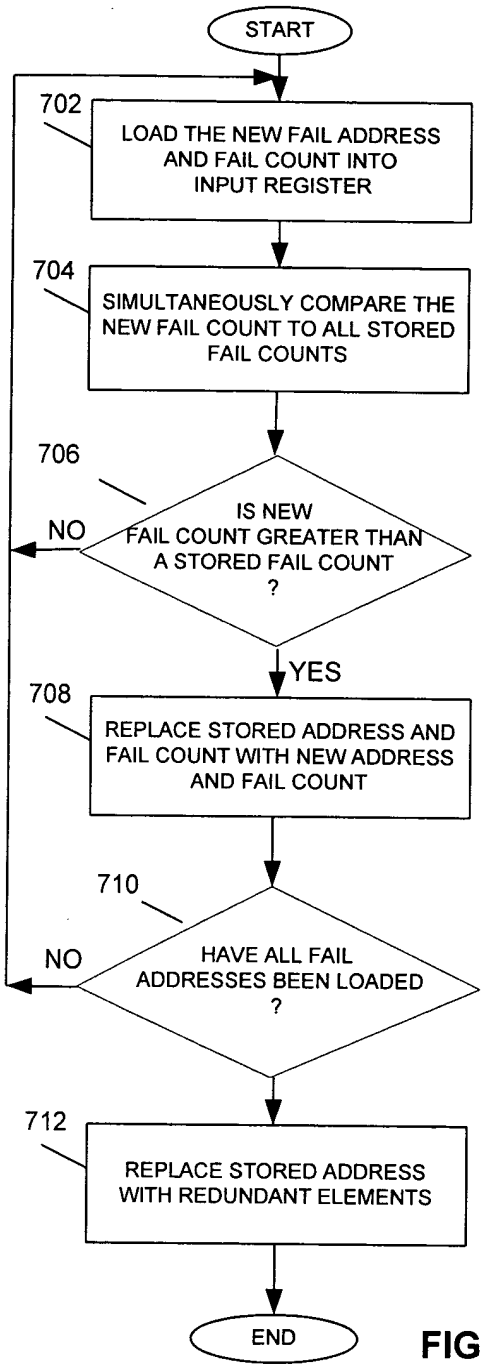
START
702
LOAD THE NEW FAIL ADDRESS AND FAIL COUNT INTO INPUT REGISTER
704
SIMULTANEOUSLY COMPARE THE NEW FAIL COUNT TO ALL STORED FAIL COUNTS
706
IS NEW FAIL COUNT GREATER THAN A STORED FAIL COUNT ?
NO
YES
708
REPLACE STORED ADDRESS AND FAIL COUNT WITH NEW ADDRESS AND FAIL COUNT
710
HAVE ALL FAIL ADDRESSES BEEN LOADED ?
NO
712
REPLACE STORED ADDRESS WITH REDUNDANT ELEMENTS
END

FIG. 7

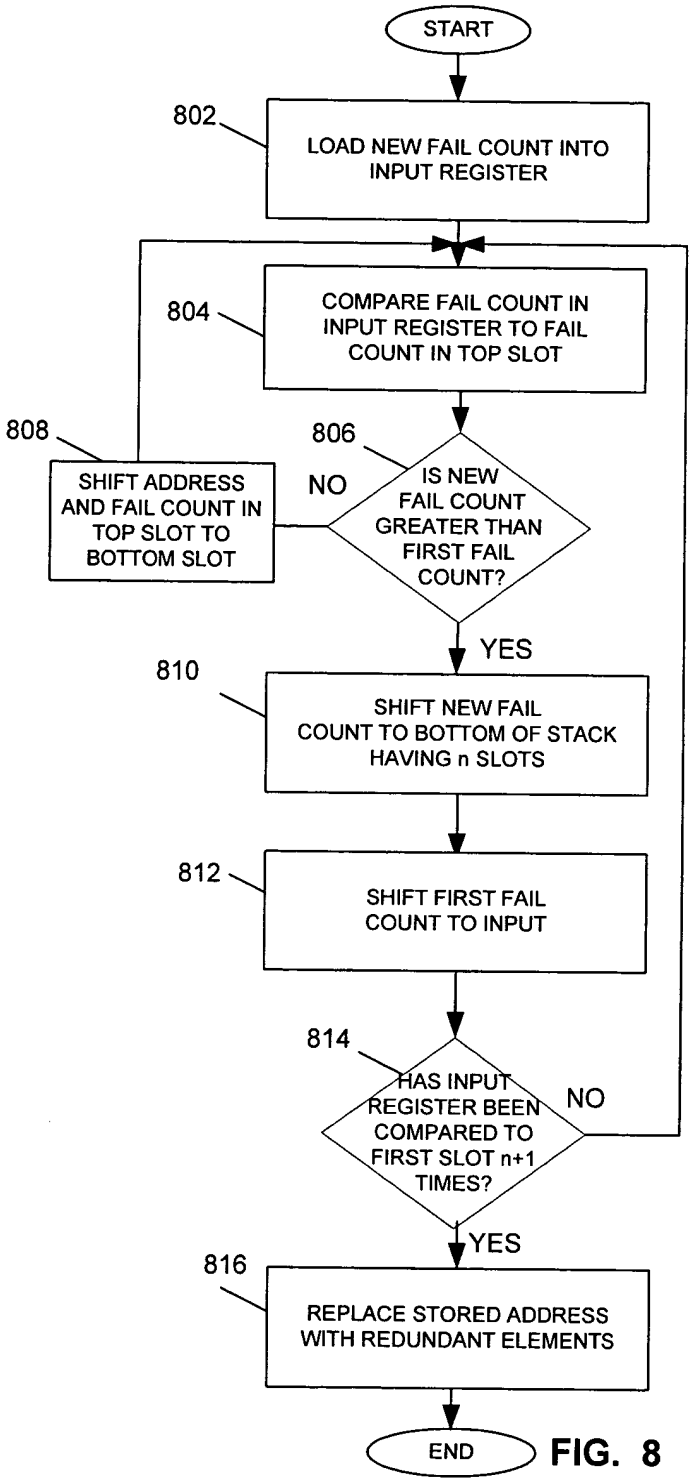
START
802
LOAD NEW FAIL COUNT INTO INPUT REGISTER
804
COMPARE FAIL COUNT IN INPUT REGISTER TO FAIL COUNT IN TOP SLOT
806
IS NEW FAIL COUNT GREATER THAN FIRST FAIL COUNT?
NO
808
SHIFT ADDRESS AND FAIL COUNT IN TOP SLOT TO BOTTOM SLOT
YES
810
SHIFT NEW FAIL COUNT TO BOTTOM OF STACK HAVING n SLOTS
812
SHIFT FIRST FAIL COUNT TO INPUT
814
HAS INPUT REGISTER BEEN COMPARED TO FIRST SLOT n+1 TIMES?
NO
YES
816
REPLACE STORED ADDRESS WITH REDUNDANT ELEMENTS
END

FIG. 8